

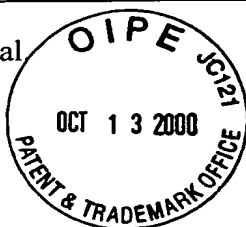
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KELKAR et al

Application No.: 09/653,925

Filed: September 01, 2000

Title: WAFER LEVEL CHIP SCALE PACKAGE



Attorney Docket No.: NSC1P181/P04767

Examiner: Unknown

Group: Not Yet Assigned

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R. Stokes

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Assistant Commissioner for Patents, Washington, DC 20231 on October 9, 2000.

Signed: 

Kristina Gomez

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR §§1.56 AND 1.97(c)

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Assistant Commissioner for Patents
Washington, DC 20231

TECHNOLOGY CENTER 2800

Dear Sir:

The references listed in the attached PTO Form 1449, copies of which are attached, may be material to examination of the above-identified patent application. Applicants submit these references in compliance with their duty of disclosure pursuant to 37 CFR §§1.56 and 1.97. The Examiner is requested to make these references of official record in this application.

This Information Disclosure Statement is not to be construed as a representation that a search has been made, that additional information material to the examination of this application does not exist, or that these references indeed constitute prior art.

This Information Disclosure Statement is being filed within three (3) months of the filing date of the above-referenced application. Accordingly, it is believed that no fees are due in connection with the filing of this Information Disclosure Statement. However, if it is determined that any fees are due, the Commissioner is hereby authorized to charge such fees to Deposit Account 50-0388 (Order No. NSC1P181).

Respectfully submitted,

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